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IN THE CLALMS

1. (original) A circuit carrier, comprising

a substrate having a surface, said surface having a passive component connecting area;

a patterned circuit layer on said surface of said substrate, said patterned circuit layer having at least a set of passive component electrode pads on said passive component connecting area, said set of passive component electrode pads including a first passive component electrode pad and a second passive component electrode pad; and

a solder mask layer covering said surface of said substrate, said solder mask layer including at least a set of solder mask openings, said set of solder mask openings including a first solder mask opening, a second solder mask opening, and a third solder mask opening, said first solder mask opening and said second solder mask opening exposing said first passive component electrode pad and said second passive component electrode pad respectively, said third solder mask opening having a length direction, said third solder mask opening along said length direction being divided into a central area, a first extension area, and a second extension area, said central area being between said first and said second solder mask openings, said first extension area and said second extension area extending from said central area along said length direction to two sides respectively, the width of said central area being smaller than the width of said first extension area.

2. (original) The circuit carrier of claim 1, wherein said circuit carrier is an IC package substrate.

3. (original) The circuit carrier of claim 1, wherein said surface of said circuit carrier includes a top surface and a bottom surface corresponding to said top surface.

4. (original) The circuit carrier of claim 1, wherein the widths of said first and second extension areas increase gradually from said central area along said length direction.

5. (original) The circuit carrier of claim 4, wherein the shape of each said first and second extension areas is a trapezoid, and the shorter side of each of said trapezoid is connected to one side of said central area along said length direction.

6. (original) The circuit carrier of claim 1, wherein the width of said first extension areas increases gradually from said central area along said length direction.

7. (withdrawn) The circuit carrier of claim 6, wherein the shape of said first extension area is a trapezoid and the shape of said second extension is a rectangle, and the shorter side of said trapezoid and the shorter side of said rectangle are connected to two sides of said central area along said length direction, respectively.

8. (original) A package structure, comprising

a circuit carrier, said circuit carrier including

a substrate having a surface, said surface having a passive component connecting area;

a patterned circuit layer on said surface of said substrate, said patterned circuit layer having at least a set of passive component electrode pads on said passive component connecting area, said set of passive component electrode pads including a first passive component electrode pad and a second passive component electrode pad; and

a solder mask layer covering said surface of said substrate, said solder mask layer including at least a set of solder mask openings, said set of solder mask openings including a first solder mask opening, a second solder mask opening, and a third solder mask opening, said first solder mask opening and said second solder mask opening exposing said first passive component electrode pad and said second passive component electrode pad respectively, said third solder mask opening having a length direction, said third solder mask opening along said length direction being divided into a central area, a first extension area, and a second extension area, said central area being between said first and said second solder mask openings, said first extension area and said second extension area extending from said central area along said length direction to two sides respectively, the width of said central area being smaller than the width of said first extension area; and

at least a passive component having a first electrode and a second electrode, said first electrode and said second electrode being soldered to said first passive component electrode pad and said second passive component electrode pad respectively.

9. (original) The package structure of claim 8, further comprising an encapsulant covering said passive component.

10. (original) The package structure of claim 8, wherein said circuit carrier is an IC package substrate.

11. (original) The package structure of claim 8, wherein said surface of said circuit carrier includes a top surface and a bottom surface corresponding to said top surface.

12. (original) The package structure of claim 8, wherein the widths of said first and second extension areas increase gradually from said central area along said length direction.

13. (original) The package structure of claim 12, wherein the shape of each said first and second extension areas is a trapezoid, and the shorter side of each of said trapezoid is connected to one side of said central area along said length direction.

14. (original) The package structure of claim 8, wherein the width of said first extension areas increases gradually from said central area along said length direction.

15. (withdrawn) The package structure of claim 14, wherein the shape of said first extension area is a trapezoid and the shape of said second extension is a rectangle, and the shorter side of said trapezoid and the shorter side of said rectangle are connected to two sides of said central area along said length direction respectively.

16. (original) The package structure of claim 8, wherein said passive component is a resistor, a capacitor, or an inductor.

No fee is believed to be due in connection with the filing of this paper. However, the Commissioner is authorized to charge any fees that may be required to Account No. 50-0710 (Order No. JCLA12583).

Respectfully submitted,
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